50 Å to 200 Å. An oxygen ashing process may be performed to oxidize the surface of silicon nitride film **135** to prevent resist poisoning.

Referring to FIG. **5**E, a positive photoresist layer **150** is applied on nitride hardmask layer **135** above the pFET regions. Positive photoresist layer **150** is used to open the nFET regions of substrate **105**. Traditional ArF or KrF lithography processes may be used.

Referring to FIG. **5**F, nitride hardmask layer **135** protecting the channel silicon germanium (SiGe) epitaxial layer **120** above the nFET regions is removed, exposing the nFET SiGe epitaxial layer **120**. Nitride hardmask layer **135** may be removed via reactive ion etch (RIE) or wet chemistry that etches nitride selective to resist, such as hydrofluoric ethylene glycol (HFEG).

Referring to FIG. **5**G, positive photoresist layer **150** is removed. Positive photoresist layer **150** may be removed using wet resist strip techniques. Sulfuric peroxide and standard clean 1 (SC-1) may be used to remove positive photoresist layer **150**.

Referring to FIG. **5**H, epitaxial layer **120** above the nFET regions is removed. Epitaxial layer **120** may be etched away using a wet etch chemistry process. Hot standard clean 1 (SC-1) may be used, such as 65 degree C., NH4OH+H2O2, to etch silicon germanium (SiGe). The time of the etch can be adjusted to ensure full removal of the silicon germanium (SiGe) epitaxial layer based on its thickness and composition. Alternative wet chemistries known to etch silicon germanium (SiGe) and may also be used.

Referring to FIG. **5**I, nitride hardmask layer **135** protecting silicon germanium (SiGe) epitaxial layer **120** above the pFET regions is removed. A hot phosphoric acid etch or HFEG etch may be used to remove nitride hardmask layer **135**.

The method as described above is used in the fabrication of integrated circuit chips. The resulting integrated circuit chips can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

The description of the present invention has been presented for purposes of illustration and description, but is not intended to be exhaustive or limited to the invention in the form disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The embodiment was chosen and described in order to best explain the principles of the invention and the practical application, and to enable others of ordinary skill in the art to understand the invention for various embodiments with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. A method of forming a device, comprising the following steps in the order named:

providing a wafer having a pad oxide layer, the wafer including a silicon substrate and having nFET regions and pFET regions;

removing the pad oxide layer to expose a silicon channel above the nFET regions and the pFET regions;

performing a wet oxide etch preclean on the silicon channel;

growing a silicon germanium (SiGe) epitaxial layer on the silicon channel, wherein the silicon germanium (SiGe) epitaxial layer is directly connected to the silicon channel and functions as part of the silicon channel;

depositing a hardmask layer on the silicon germanium (SiGe) epitaxial layer;

applying a positive photoresist layer on the hardmask layer above the pFET regions;

removing the hardmask layer above the nFET regions;

removing the positive photoresist layer;

removing the silicon germanium (SiGe) epitaxial layer above the nFET regions; and

removing the hardmask layer above the pFET regions.

2. A method according to claim **1**, wherein the hardmask layer comprises a deposited oxide film.

3. A method according to claim **2**, wherein the deposited oxide film is deposited by rapid thermal chemical vapor deposition (RTCVD), low pressure chemical vapor deposition (LPCVD), sub-atmospheric chemical vapor deposition (SACVD) or atomic layer deposition (ALD).

4. A method according to claim **3**, wherein the deposited oxide film has a thickness of approximately 10 Å to 200 Å.

5. A method according to claim **1**, wherein the hardmask layer comprises a nitride hardmask.

6. A method according to claim **5**, wherein the nitride hardmask is deposited by low pressure chemical vapor deposition (LPCVD), rapid thermal chemical vapor deposition (RTCVD) or atomic layer deposition (ALD).

7. A method of forming a device, comprising the following steps in the order named:

providing a wafer having a pad oxide layer, the wafer including a silicon substrate and having nFET regions and pFET regions;

removing the pad oxide layer to expose a silicon channel above the nFET regions and the pFET regions;

performing a wet oxide etch preclean on the silicon channel;

growing a silicon germanium (SiGe) epitaxial layer on the silicon channel, wherein the silicon germanium (SiGe) epitaxial layer is directly connected to the silicon channel and functions as part of the silicon channel;

depositing a first hardmask layer on the silicon germanium (SiGe) epitaxial layer;

depositing a second hardmask layer on the first hardmask layer;

applying a positive photoresist layer on the second hardmask layer above the pFET regions;

removing the second hardmask layer above the nFET regions;

removing the positive photoresist layer;

removing the first hardmask layer above the nFET regions;

removing the silicon germanium (SiGe) epitaxial layer above the nFET regions;

removing the second hardmask layer above the pFET regions; and

removing the first hardmask layer above the pFET regions.

8. A method according to claim **7**, wherein the first hardmask layer comprises a deposited oxide film.

9. A method according to claim **7**, wherein the second hardmask layer comprises a silicon nitride film.

10. A method according to claim **9**, wherein the silicon nitride film is deposited via low pressure chemical vapor